**Amendments to the Claims:**

1. (Previously Presented) An apparatus for segmenting variable length packet and forming fixed cell therefrom comprising:
a storage unit, with storage capacity greater than storage capacity of a one byte register, for storing the variable length packet;
a storage control block for storing segmenting information;
a bus connected to an external interface to request and receive acknowledgment of segmenting information availability;
a first input data bus connected to the storage control block to read the segmenting information;
a second input data bus connected to the storage unit to read predefined portions of said variable length data packet to be used to form the fixed cell;
a multiplexer having two inputs with one of said two inputs connected to the first input data bus and the other of said two inputs connected to the second input data bus wherein the data packets used to form the fixed cell are extracted directly from the storage and not buffered in a register connected between the storage and said multiplexor;
a counter having an input connected to the storage control block and an output connected to the storage unit, said counter pointing to the next address in the word of the packet to be read in the storage unit;
a finite state machine having an input connected to the storage control block, a first output connected to the counter and a second output connected to the multiplexer said finite state machine, for each cell to be built, requesting and receiving acknowledgment, over said bus connected to said external interface, of segmenting information availability, repetitively activating said multiplexer with storage unit data and segmenting information data according to a finite cell pattern and sending cell data on said output bus to said cell output while incrementing said counter until said output cell is complete; said finite state machine repetitively outputting cells according to said cell pattern until all the packet words are read.

2. (Original) The apparatus of claim 1 further comprising two buses connected to a storage unit controller controlling said storage unit, one bus being connected to the counter and sending the address to read in the storage unit and one bus connected to the finite state machine to send request for data availability on the multiplexer first input bus reading and to receive acknowledgment for storage unit data availability on the multiplexer first input bus.

3. (Original) The apparatus of claim 1 wherein the control block comprises the packet header and the cell header having respectively 6 unit and 10 unit length, said finite state machine activating said multiplexer with said headers and storage unit data to build the cells according to said cell pattern.

4. (Original) The apparatus of claim 1 wherein, the control block comprises a data field having an even length to be replaced in the packet so that said finite state machine activates said multiplexer with said data field and storage unit data to build the cells with the replaced field according to said cell pattern.

5. (Original) The apparatus of claim 1 wherein, the control block comprises a data field having an even length to be inserted in the packet, so that said finite state machine activates said multiplexer with said data field and storage unit data to build the cells with the inserted field according to a cell pattern with a different cell order than the cell pattern used when no data field is inserted in the packet.

6. (Original) The apparatus of claim 1 wherein the counter is read from the segmenting information at each new cell and incremented by said finite state machine, modulo the storage unit word length, of the length of said cell data sent on said output bus.

7. (Original) The apparatus of claim 1 wherein said storage unit word length is 16 bytes, said multiplexer output bus is a 4 byte bus and said cell fixed length is 64 bytes, said output cell being filled by 16 clock cycles sequencing said finite state machine, with 4 bytes at each clock cycle.

8. (Previously Presented) A method to assemble fixed size cell:
providing a storage unit, with storage capacity greater than storage capacity of a one byte register, for storing the variable length packet;
providing a storage control block for storing segmenting information;
requesting and receiving acknowledgment of segmenting information availability on a bus connected to an external interface;
reading the segmenting information on a first input data bus connected to the control block;
reading the variable length packet data on a second input data bus connected to the storage unit;
requesting and receiving acknowledgment, over a bus interconnecting a Finite State Machine to an external interface of segmenting information availability;
repetitively activating a multiplexer having as inputs said two input data buses according to a cell pattern and sending cell data on a output bus of said multiplexer to said output cell while incrementing a counter pointing to the next address in the word of the packet to be read in the storage unit, until said output cell is complete.

9. (Previously presented) The method of claim 8 further comprising:
requesting availability of said storage unit data on said first input bus by sending a signal via a signal bus to a storage unit controller and by sending the counter address where to read said storage unit via one other bus; and,
receiving an acknowledgment for storage unit data availability via said signal bus.

10. (Previously presented) The method of claim 8 further comprising activating said multiplexer with cell header and packet header, having respectively 6 unit and 10 unit length, stored in said storage control block and available on said second input bus and sending the data on said output bus according to said cell pattern.

11. (Currently Amended) The method of claim 8 further comprising activating said multiplexer with an even length field stored in said control block, available on said first input bus to replace a same length field in the packet data to be stored in the [[the]]cell according to said cell pattern.

12. (Previously presented) The method of claim 8 further comprising activating said multiplexer with an even length field stored in said control block, available on said first input bus to be inserted in the packet data to be stored in the cell according to said cell pattern; said cell pattern being differently ordered than the cell pattern used when no data field is to be inserted in the packet data.

13. (Previously presented) The method of claim 8 further comprising reading the counter value in the segmenting information at each new cell and wherein said incrementing step is done, modulo said storage unit packet word length, with the length of said cell data sent on said output bus.

14. (Original) The method of claim 8 wherein said storage unit word length is 16 bytes, said multiplexer output bus is a 4 byte bus and said cell fixed length is 64 bytes.

15. (Currently Amended) An adapter in a network equipment comprising:
input ports receiving network variable length data packets;
a frame process component storing as words said data packets in a storage unit, creating queues of packet going to the same destination address and creating control blocks with packet information;
a scheduler designating a packet queue to be served at a given time; and
a packet segmenting process component preparing ~~the~~ segmenting information for assembling each ~~restore 64 unit~~ fixed length cell from packets in packet queues ~~result of the segmenting of the packet to be served in the designated queue~~.

16. (Currently Amended) ~~The adapter of claim 15 wherein~~ An adapter in a network equipment comprising:
input ports receiving network variable length data packets;
a frame process component storing as words said data packets in a storage unit creating queues of packet going to the same destination address and creating control blocks with packet information;
a scheduler designating a packet queue to be served at a given time; and
a packet segmenting process component preparing segmenting information for assembling each 64 unit fixed length cell from packets in packet queues the packet segmenting process component comprising ~~comprises~~:

a storage unit, with storage capacity greater than storage capacity of a one byte register, for storing the variable length packet;
a storage control block for storing segmenting information;
a bus connected to an external interface to request and receive acknowledgment of segmenting information availability;
a first input data bus connected to the storage control block to read the segmenting information;

a second input data bus connected to the storage unit to read said variable length data packet;
a multiplexor having as inputs the two said input data buses and an output bus;
a counter pointing to the next address in the word of the packet to be read in the storage unit;
a finite state machine, for each cell to be built, requesting and receiving acknowledgment of segmenting information availability, repetitively activating said multiplexer with storage unit data and segmenting information data according to a finite cell pattern and sending cell data on said output bus while incrementing said counter until said output cell is completed; said finite state machine repetitively filling said output cells according to said cell pattern and until all the packet words are read.

17. (Previously presented) The method of claim 8 further including repetitively completing cells by repeating the previous steps and until all the packet words are read.

18. (New) The adapter of claim 15 wherein each fixed length cell includes 64 units.

19. (New) The adapter of claim 15 or 18 further including cell assembler component using the segmenting information to segment the packet in the queue selected by the scheduler.